IN THE CLAIMS

1. (Cancel)

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9. (Currently amended) A buffer management system for controlling access to a buffer, comprising

a buffer manager that is configured to assert a wrap signal when a first buffer operation involves consecutively accessing each buffer location of a block of buffer locations assigned sequential address values in an order different than an order defined by the sequential address values ~~to the buffer is non-sequential~~, and is further configured to limit accesses to the buffer of a second ~~access to the~~ buffer operation in dependence upon the wrap signal.

10. (Currently amended) The buffer management system of claim 9, wherein

the first ~~access to the~~ buffer operation includes an access that is based on a block address and an offset address, and

the second ~~access to the~~ buffer operation is limited to the block address when the wrap signal is asserted, and is limited to a combination of the block address and the offset address when the wrap signal is deasserted.

11. (Previously presented) The buffer management system of claim 10, wherein

a change of limit of the second access is communicated via a gray-code sequence.

12. (Currently amended) The buffer management system of claim 10, wherein

the buffer manager is further configured to assert an idle signal when the first ~~access to the~~ buffer operation terminates, and

the second ~~access to the~~ buffer operation is further limited to the block address when the idle signal is asserted.

13. (Currently amended) The buffer management system of claim 9, wherein

the first access and the second ~~access~~ buffer operations correspond to:

a series of write-accesses to the buffer, and

a series of read-accesses to the buffer.

14. (Currently amended) A method of controlling access to a buffer comprising:

determining a block address and an offset address corresponding to a first ~~access to the~~ buffer operation involving consecutively accessing each buffer location of a block of buffer locations assigned sequential block address values,

determining when the offset address is non-sequential relative to the block address wherein the buffer locations are accessed in an order different than an order defined by the sequential address values, and

limiting access of a second ~~access to the~~ buffer operation to ~~the block address~~locations within the block when the offset address is non-sequential.

15. (Currently amended) The method of claim 14, further including:

determining when the offset address is sequential relative to the block address, and

limiting accesses of the second ~~access to the~~ buffer operation to a combination of the block address and the offset address when the offset address is sequential.

16. (Currently amended) The method of claim 14, wherein

limiting the accesses of the second ~~access~~ buffer operation includes determining a gray-code sequence corresponding to a change in the block address.